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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/847,667	05/01/2001	Subhash Gupta	54364	4777

7590 01/10/2005

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EXAMINER
MITCHELL, JAMES M

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 01/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/847,667	GUPTA ET AL.	
	Examiner	Art Unit	
	James M. Mitchell	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) *11-16* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the request for continued examination filed October 25, 2004.

Allowable Subject Matter

2 The indicated allowability of claims is withdrawn in view of the newly discovered reference(s) to Gaul (U.S. 5,646,067). Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 3-9 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by a Gaul (U.S 5,646,067).

5. Gaul discloses (Fig 1A-K) discloses an integrated circuit comprising a wafer material having first and second surfaces (top most surface and bottom portions, 111), said substrate comprising a circuit layer (119) comprising integrated circuit elements and a substrate (111) that lacks integrated circuit elements adjacent to said circuit layer (119), said circuit layer being located between said first surface layer and said substrate layer (portion of 111, beneath item 119), a plurality of via (132; also shown in Fig 3) extending from said first substrate through said circuit layer and into said substrate layer said vias having a bottom surface comprising a stop material (134) more resistant to

removal by polishing than said wafer material (Fig 2B-2C); (cl. 3,4) where the vias are lined with an electrically insulating silicon dioxide material (Col. 3, Line 13); (cl.5, 6) and the vias are filled with an electrically conducting material (137) of tungsten (Col. 5, Line 57); (cl. 8, 9) and further disclosing vias filled terminating in an electrically conducting pad (Fig 4P; Col. 11, Lines 1-11 and the pad extends above a dielectric layer (i.e.134, 151,311).

6. Claims 1-3 and 5 are rejected under 35 U.S.C. 102(b) as being anticipated by Gradinger (U.S 5,229,647).

7. Gradinger discloses (Fig 4, 5, 6) discloses an integrated circuit comprising a wafer material (10) having first and second surfaces (top most surface and bottom portions), said substrate comprising a circuit layer (119) comprising integrated circuit elements and a substrate (lower portion of 10 away from pad, 23, 25) that lacks integrated circuit elements adjacent to said circuit layer (i.e. "integrated circuit"), said circuit layer being located between said first surface layer and said substrate layer, a plurality of via (42) extending from said first substrate through said circuit layer and into said substrate layer said vias having a bottom surface (i.e. farthest point form pad) comprising a SiN stop material (23) more resistant to removal by polishing than said wafer material (as admitted by applicant's claim 2); (cl. 5, 8, 9) and further disclosing vias filled (20) terminating in an electrically conducting pad (25) that extends above a dielectric layer ("OX."; Fig 5)

8. Claims 1-3, 5, 8 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Clements (U.S 4,954,875).

9. Clemets discloses (Fig 4, 5, 6) discloses an integrated circuit comprising a wafer material (10) having first and second surfaces (top most surface and bottom portions), said substrate comprising a circuit layer (Col. 1, Lines 26-27; Col. 8, Lines 56-57) comprising integrated circuit elements and a substrate that lacks integrated circuit elements adjacent to said circuit layer (i.e. "integrated circuit"), said circuit layer being located between said first surface layer and said substrate layer, a plurality of via (Fig 1, 25) extending from said first substrate through said circuit layer and into said substrate layer said vias having a bottom surface (i.e. farthest point form pad; Fig 12) comprising a SiN stop material (Fig 9, 40)that is more resistant to removal by polishing than said wafer material (as admitted by applicant's claim 2); (cl. 5) and further disclosing vias filled (26) terminating in an electrically conducting pad (33).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gaul (U.S. 5,646,067).

12. Gaul discloses the elements of paragraph 5 of this office action and further an thickness for the circuit layer, but does not appear to show the thickness of the circuit layer between 4 and 9 microns. In any case, it would have been an obvious matter of

design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

13. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gaul (U.S 5,646,067) as applied to claim 1 and further in combination with MORI et al. (U.S. 2001/0045652).

14. Gaul discloses the use of a TiN barrier and that other barrier layers may by used (Col. 5, Lines 20-24), but does not disclose for example Ta or Tan.

15. MORI shows that TiN or Tare equivalent barrier layers known in the art known in the art. Therefore, because these two barrier layers are art recognized equivalents at the time the invention was made, one of ordinary skill in the art would have found it obvious to substitute a Ta for TiN.

Conclusion

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James M. Mitchell whose telephone number is (571) 272-1931. The examiner can normally be reached on M-F 8:00-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jmm
January 5, 2004

Craig A. Thompson

CRAIG A. THOMPSON
PRIMARY EXAMINER